REMARKS/ARGUMENTS

This Amendment is responsive to the Office Action mailed on May 17, 2005. In this Amendment, claims 9, 10, and 12 are amended, claims 15 and 17 are canceled, and claims 22-23 are added so that claims 9-10, 12-14, 16, and 18-23 are pending and subject to examination.

I. Claim rejections - 35 USC 103

A. Mahulikar et al. and Davis et al.

Claims 9, 10, 12-15, 18, 20 and 21 are rejected as being obvious over Mahulikar et al. (US 5,629,835 hereinafter "Mahulikar et al.") and Davis et al. (US 5,814,884 hereinafter "Davis et al."). This rejection is traversed.

Obviousness has not been established, since all limitations of claim 9 are not taught or suggested by the cited art. To establish *prima facie* obviousness, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 580 (CCPA 1974). MPEP 2143.01. Here, neither Mahulikar et al. nor Davis et al. teach or suggest a method for making a chip device comprising, *inter alia*, placing solder balls into the dimples of a leadframe, and attaching a die to the leadframe, wherein a first surface of the die including a drain connection is electrically coupled to a major surface of the leadframe, where the major surface defines at least part of the die attach cavity. Referring to FIGS. 1 and 2 of the present application, a die 13 can be attached to a leadframe 10 and placed in a die attach cavity 11. As explained at page 3, lines 6-10, the solder balls 22 in the dimples 12 of the leadframe 10 can be electrically connected to a drain region of the die while solder bumps 21 on the die 13 are connected to source and gate regions in the die 13. Thus, in embodiments of the invention, the device in the die 13 has an input at one side of the die 13 (through solder bumps 21) an output at the other side of the die 13 (which connects to the leadframe 10 and solder balls 22).

Mahulikar et al. is cited as teaching the steps in the method of claim 9, with the exception of a MOSFET (see page 2 of the Office Action). Referring to FIG. 9 of Mahulikar et al., Mahulikar et al. discloses a semiconductor device 54 which is bonded to the central portion of a base 62 via a die attach 56 (col. 7 lines 27-28 of Mahulikar et al.). As noted at col. 6, lines 55-57, "[i]f the base 62 is electrically conductive, the base is coated with an electrically insulating layer 64". A brief review of Mahulikar et al.'s figures also shows that the other embodiments that are disclosed have a base with an electrically insulating layer around a conductive portion. Because there is an electrically insulating layer 64 covering any conductive part of the base 62, Mahulikar et al. does **not** electrically couple the side of the semiconductor device 54 facing the major surface of the base 62 to the base 62.

It would not have been obvious to have modified Mahulikar et al. to arrive at the invention of independent claim 9, with or without the teachings in Davis et al., since doing so would be contrary to the intended purpose of Mahulikar et al.'s invention. If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 221 USPQ 1125 (Fed. Cir. 1984). MPEP § 2143.01. As noted above, Mahulikar et al. discloses an insulating layer 64 in a base 62. In order for Mahulikar et al.'s semiconductor device to electrically couple to the base 62 (pursuant to claim 9), it is necessary to remove the insulating layer 64. Col. 6, lines 58-65 of Mahulikar et al. suggests that the insulating layer 64 is necessary to prevent a short circuit between any solder balls on the base 62. Put another way, referring to FIG. 9 of Mahulikar et al., if the insulating layer 64 was not present, then the solder balls 70 would undesirably short circuit. Accordingly, if one were to remove the insulating layer 64 from Mahulikar et al.'s base, this would be contrary to Mahulikar et al.'s intended purpose.

B. Mahulikar et al., Davis et al., and DiStefano et al.

Claim 17 is rejected as obvious over Mahulikar et al., Davis et al., and in further view of DiStefano et al. (US 6,458,681 hereinafter "DiStefano et al."). The Examiner states that DiStefano et al. teaches a method of making a chip device wherein the die has solder balls

thereon (page 4 of the Office Action). Applicants submit that the additional citation of DiStefano et al. fails to remedy the deficiencies of Mahulikar et al. and Davis et al.

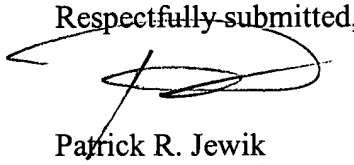
C. Advantages provided by embodiments of the invention

As explained on page 2 of the specification, embodiments of the present invention provide for a number of advantages not taught or suggested by the prior art. For example, embodiments of the invention provide for a thinner device, thereby allowing for miniaturization. The method according to an embodiment of the invention is also simplified when compared to conventional assembly processes. For example, in an embodiment of the invention, wire bonding, molding, forming, and plating may all be eliminated. In addition, the thermal performance of the resulting package is also improved as heat is dissipated from both surfaces of the die. The cited prior art references, in addition to failing to teach or suggest all of the claim limitations, fail to teach or suggest the combination of advantages provided by embodiments of the invention. Accordingly, there are many more reasons why one would conclude that the claims are patentable rather than unpatentable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned.

Respectfully submitted,



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